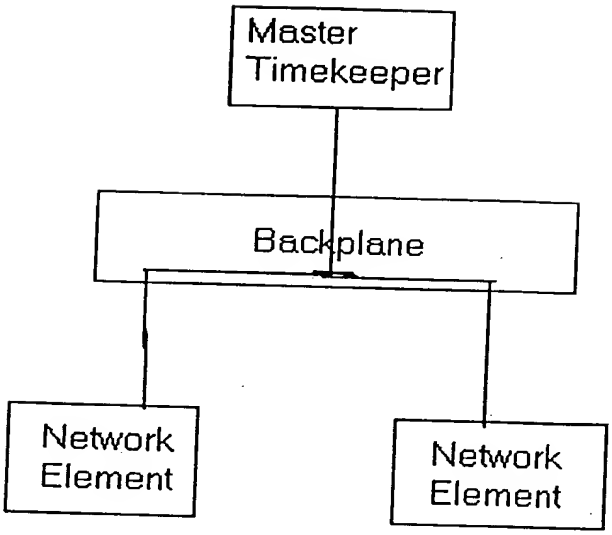

Figure 1

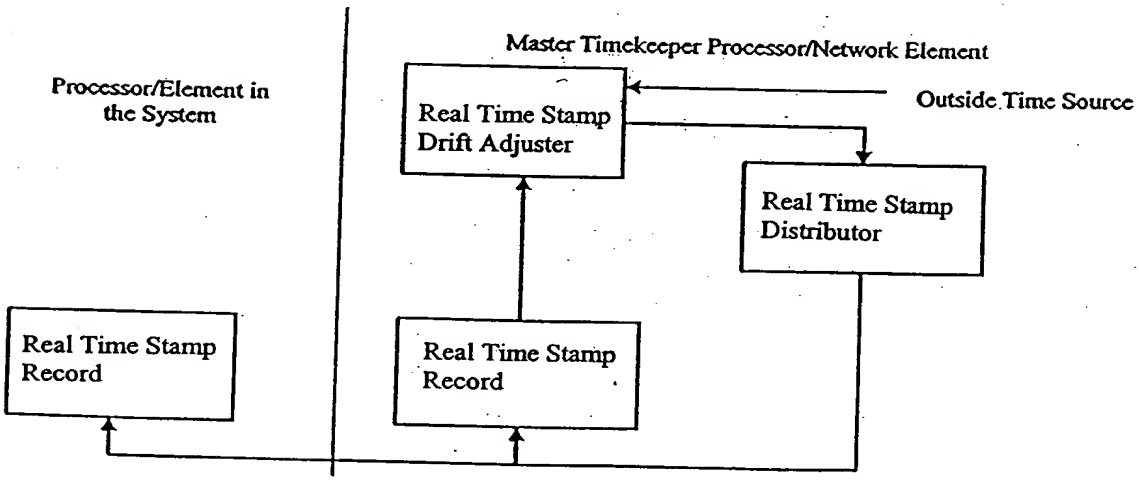

Figure 2

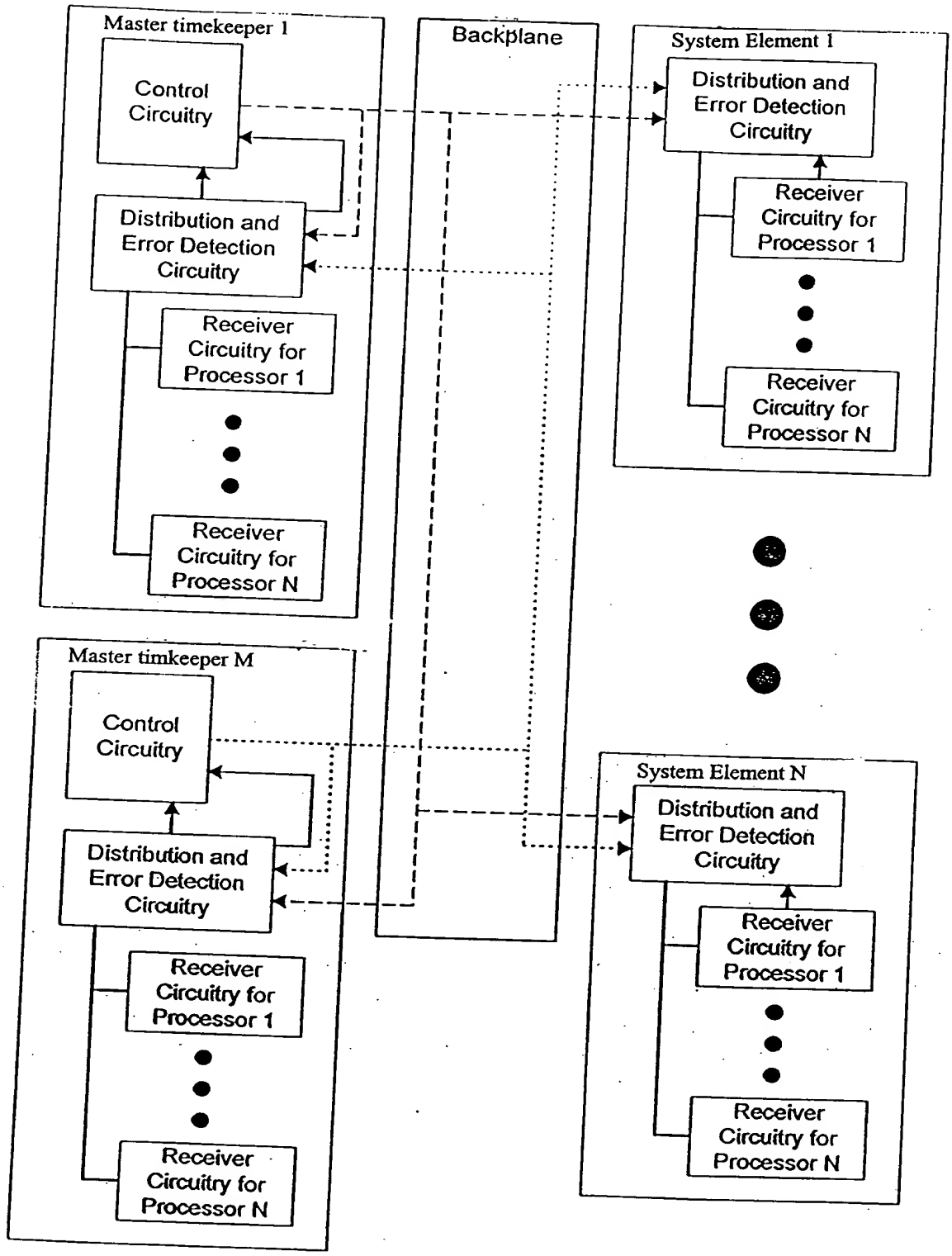
Master timekeeper 1
Control Circuitry
Distribution and Error Detection Circuitry
Receiver Circuitry for Processor 1
Receiver Circuitry for Processor N
Backplane
System Element 1
Distribution and Error Detection Circuitry
Receiver Circuitry for Processor 1
Receiver Circuitry for Processor N
Master timkeeper M
Control Circuitry
Distribution and Error Detection Circuitry
Receiver Circuitry for Processor 1
Receiver Circuitry for Processor N
System Element N
Distribution and Error Detection Circuitry
Receiver Circuitry for Processor 1
Receiver Circuitry for Processor N

Figure 3

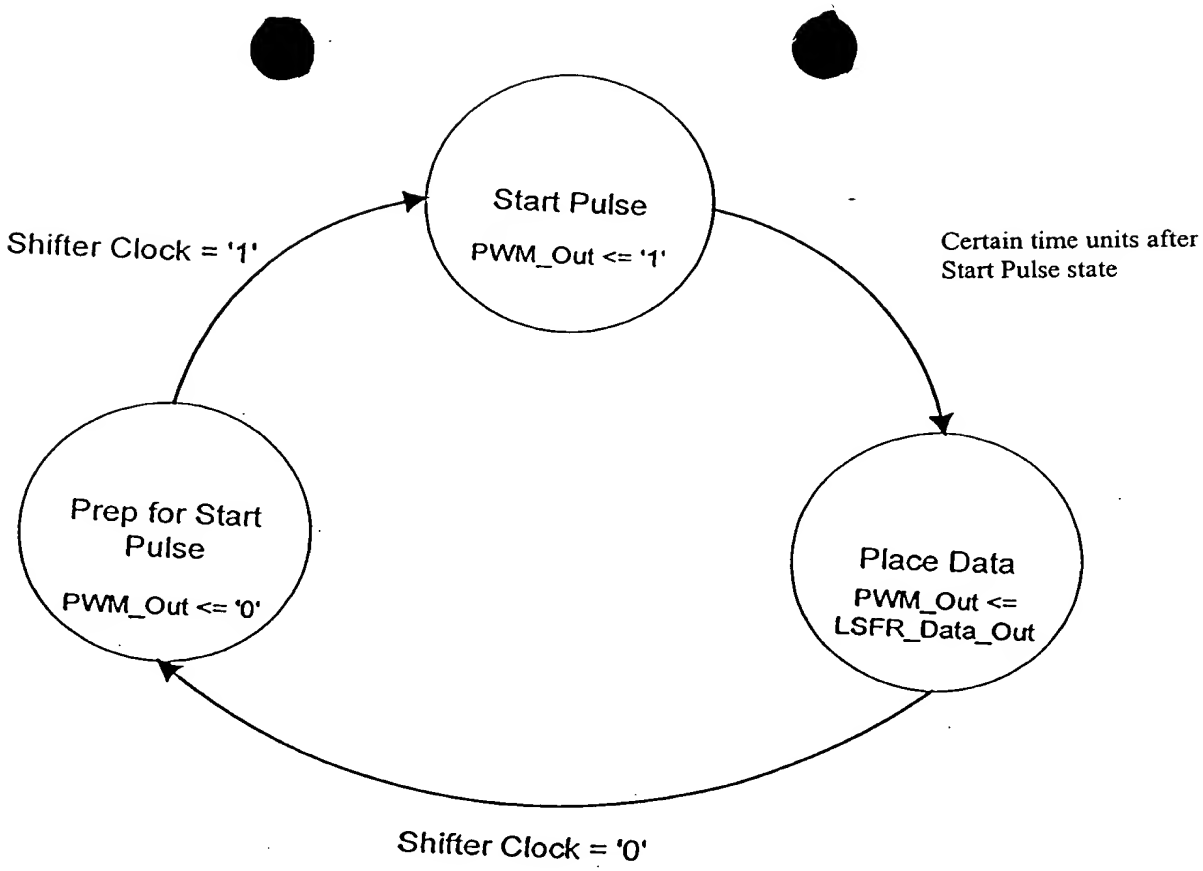

Figure 4

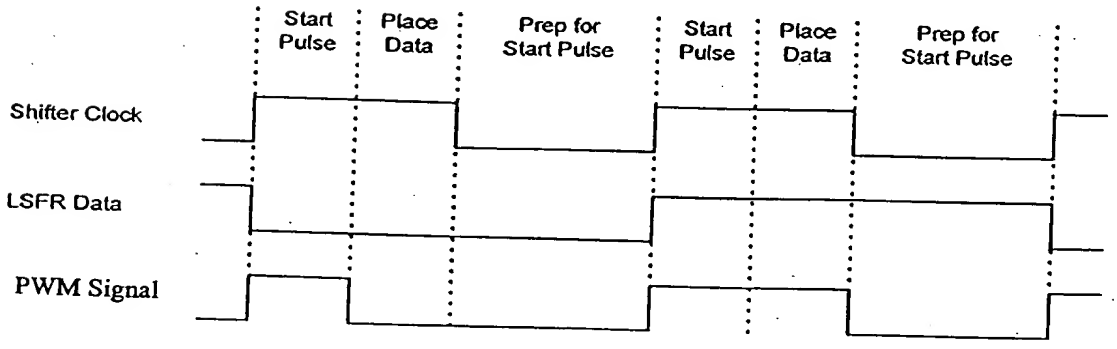

Figure 5

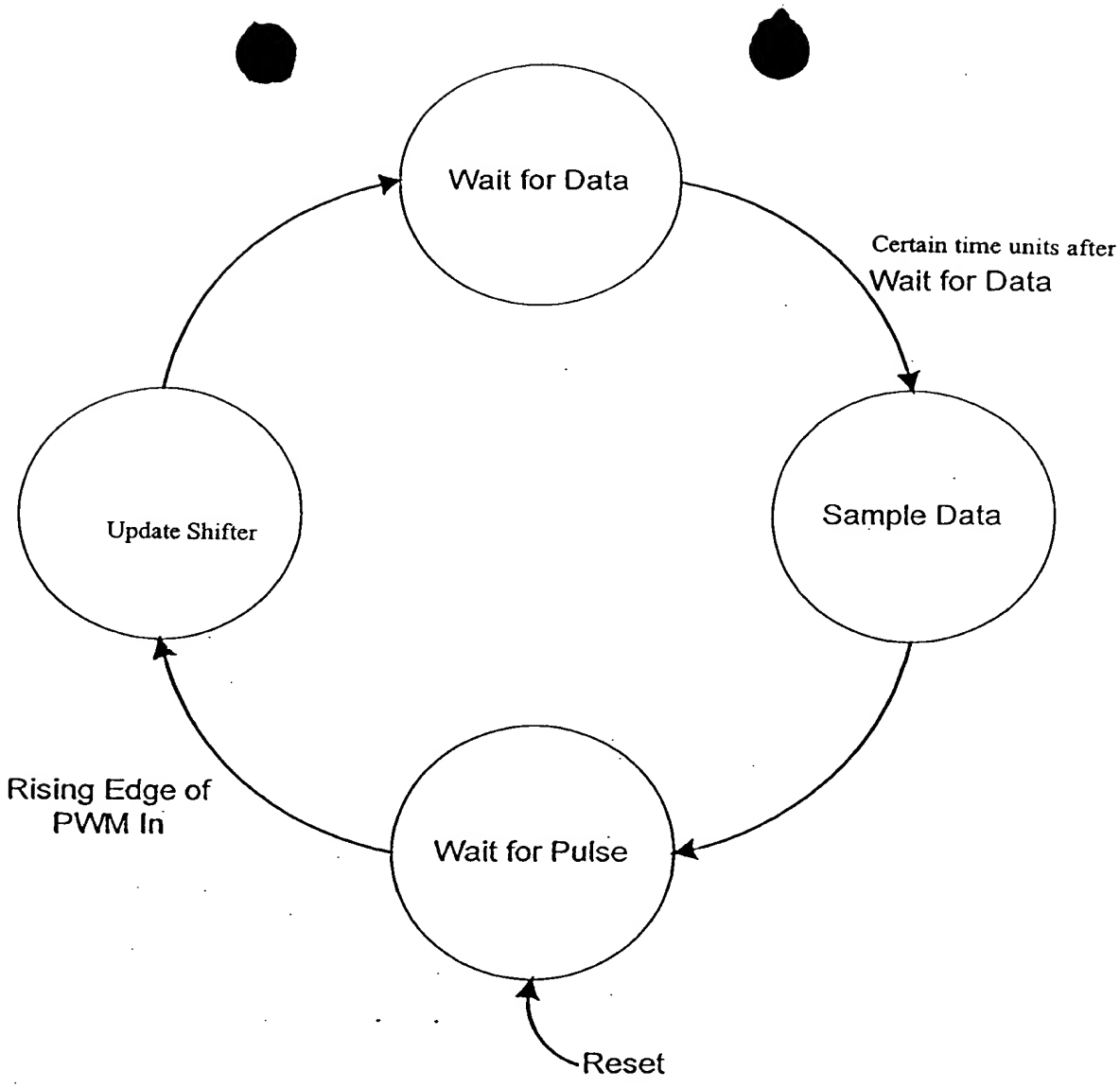

Figure 6

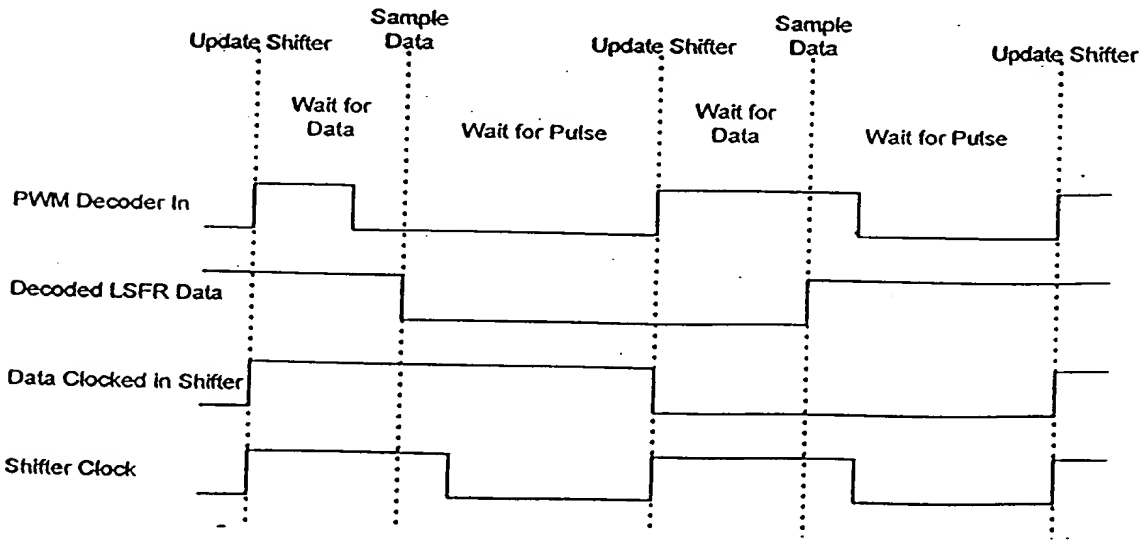

Figure 7